UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,113	12/12/2003	Ramesh G. Illikkal	42P17961	1906

7590 01/17/2006

Anthony H. Azure
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025

EXAMINER	
GU, SHAWN X	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 01/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/735,113	ILLIKKAL ET AL.	
	Examiner	Art Unit	
	Shawn Gu	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 3, 4, 6, 7, and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As for claim 1, the claim recites the limitation "the computer system" in line 4 of the claim. There is insufficient antecedent basis for this limitation in the claim. The phrase "a computer system" is more appropriate.

As for claims 3 and 4, the claims recite the limitation "the plurality of processors" in line 1 of each claim. There is insufficient antecedent basis for this limitation in the claims.

As for claim 6, the Examiner is unclear of the exact meaning of the claim language. It seems the claim is stating the first data block is received at an I/O device, but the claim contains either typographical or grammatical errors that renders the language vague and indefinite. Appropriate correction is required.

As for claim 7, the claim recites the limitation "the I/O device" in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

As for claim 16, it is unclear to the Examiner whether the plurality of processors are coupled respectively to each of the plurality of NICs, or each processor is coupled to each of the NICs. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 and 6-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sano et al. [US 6,912,602 B2] (hereinafter "Sano"), in further view of Patterson et al. [Computer Architecture A Quantitative Approach] (hereinafter "Patterson").

As for claims 1, 8, 12, and 16, Sano teaches a computer system (Fig 1), comprising:

a plurality of network interface cards (NICs) (Fig 1, 20A-C; Col 2, Lines 59-67; Col 3, Lines 1-32);

a plurality of processors communicatively coupled to each of the plurality of NICs (Fig 1, 12A-N; Col 2, Lines 55-57); and

a storage device operatively coupled to the plurality of processors, the storage device including a plurality of instructions which when executed by a processor of the plurality of processors perform operations comprising:

creating a first descriptor to correspond to a first packet; and placing the first descriptor in a descriptor ring (Col 13, Lines 65-67; Col 14, Lines 1-67; Col 15, Lines 1-42; the software must be stored in some storage device such as Memory 24 in order to be loaded and executed by the processors). Sano does not teach that the first descriptor is placed in a descriptor ring according to a striping policy to prevent false sharing of the cache line of the computer system.

However, Patterson teaches that a computing system, especially one with multi-processors having a common shared memory would benefit from having multiple memory banks for the shared memory in order to allow multiple independent accesses and also allow the CPU to proceed beyond a cache miss, potentially allowing multiple cache misses to be service simultaneously, (Page 434, last paragraph; Page 435, Line 1), and further teaches a memory design (Modulo Interleaved Memory Banks, Page 435-437) for multi-processor computer systems (Page 435, Line 11) wherein memory words are striped (interleaved) among memory banks according to the relationships disclosed on Page 436, in order to avoid memory bank conflicts. Memory word size and

cache line size are matters of design choice, and it would have been obvious to one ordinarily skilled in the art that the word size in Sano and Patterson's teachings can be defined as 16 bytes, which is also the size of Sano's descriptor, and the cache line size can be 48 bytes. As a result, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that Sano's shared memory could be implemented as multiple memory banks according to Patterson's teaching using Modulo Interleaved Memory Bank design in order to allow multiple independent accesses for memory data and avoid memory bank conflicts. Also as a direct result of the combined teachings, Sano's descriptors would be interleaved among the memory banks like all other memory data as depicted in Patterson's Figure 5.34 on Page 437. It would have also been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that a further result of this combined teaching would be placing a first descriptor in a descriptor ring (which is formed by the descriptors in the multi-banked memory as disclosed by Sano, Col 13, Lines 43-58) to prevent false sharing of a cache line of the computer system. For illustration purposes, assume the descriptors 0-23 are placed in the 3 memory banks as shown in the Module Interleaved section of Figure 5.34 on Page 437 of Patterson, then descriptors 0, 16, and 8 will be read into a cache line of 48 bytes long when processor 1 (one of Sano's plurality of processors) requests and processes descriptor 0. If processor 2 of the plurality of processors sequentially requests the next descriptor, then descriptors 9, 1, and 17 would be read into a cache line, and processor 3 would access descriptors 18, 10, and 2 in one cache line. Therefore false sharing of a cache line is prevented as a direct result of the combined

teaches of Sano and Patterson, although the motivation to combine was derived from the need to allow multiple independent accesses, allow the CPU to proceed beyond a cache miss, potentially allowing multiple cache misses to be service simultaneously, and to avoid bank conflicts.

It can be seen that the articles of manufacture in claims 8 and 12 are described above, and the method of claim 1 is clearly performed by the computer system of claim 16, wherein the first data block is the first packet of claim 16. For claim 8, there must be a first receive buffer to store the first packet received at a NIC (Sano, Col 2, Lines 59-67; Col 3, Lines 1-4; Col 6, Lines 38-41; Fig 2, 40 PDI; Fig 2, IVC0-15), and the first descriptor is created corresponding to the first receive buffer (Sano, Fig 8). For claim 12, the first descriptor is created corresponding to a first packet to be transmitted by a NIC (Sano, Col 3, Lines 58-67; Col 4, Lines 1-2; Col 13, Lines 65-67; Col 14, Lines 1-17; Fig 9, 130-136)

As for claims 2, 9, 13, and 17, Sano in combination of Patterson already substantially disclose the claim as described above, and according to the combined teachings described above, the striping policy (Patterson, Page 437, Figure 5.34, Module Interleaved) comprises placing the first descriptor (Address 1 in Modulo Interleaved Memory Bank, which is mapped to address 1 of memory bank 1) in the descriptor ring wherein the first descriptor and a second descriptor (Address 0 in Module Interleaved Memory Bank, mapped to address 0 of memory bank 0) in the

descriptor ring to not share the cache line (it is apparent from Figure 5.34 that they do not share the same cache line, as they are on different address rows of the memory banks) when the second descriptor is requested, the first descriptor to be the next descriptor requested from the descriptor ring after the second descriptor (descriptor 1 is requested after descriptor 0).

As for claims 3, 10, 14, and 18, Sano in combination of Patterson already substantially disclose the claim as described above, but neither references specifically discloses that the first descriptor is assigned to a processor of the plurality of processors according the relationship of Processor Assignment = Descriptor_Position mod N. However, Patterson discloses the address to memory bank mapping uses the relationship of Bank number = Address MOD Number of banks (Page 436), in order to avoid bank conflicts. If Sano's descriptors are assigned to the memory banks as described above, then this relationship is used. It is also obvious that Sano's plurality of processors 1-N can be any arbitrary number, and the choice of 1-N sequencing is simply a design choice that can be replaced by 0 to N-1 instead. If N is taken to be 3, and the 3 processors (processor 0 to 2) process the packets sequentially, then it is an apparent result that the processor assignment of the descriptors also uses the relationship described above, except "Bank Number" is replaced by "Processor Assignment", "Address" is replaced by "Descriptor_Position", and "Number of Banks" is replaced by "N". Therefore it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that in order for a number of processor equal to

the number of memory banks to sequentially access the descriptors stored within the memory banks according to the combined teachings of Sano and Patterson, the processor assignment relationship Processor Assignment = Descriptor_Position mod N is used.

As for claim 4, Sano further teaches the plurality of processors share a cache line (Fig 1, 24 Memory; Col 5, Lines 4-29), wherein the cache line is longer than the first descriptor (Col 11, Lines 26-28; Col 11, Lines 64-67; Col 12, Lines 1-5).

As for claims 6 and 19, Sano in combination of Patterson already substantially disclose the claim as described above, and Sano further discloses the packets are processed by software executed by the processors (Col 3, Lines 55-58). Also, NIC device driver software must be loaded in the memory and executed by the processors in order to control the operation of the NICs, which includes receiving the first packet at a NIC of the plurality of NICs.

As for claims 7 and 20, Sano further teaches that the execution of the plurality of instructions further perform operations comprising preparing the first packet at the computer system, the first packet to be transmitted from a NIC of the plurality of NICs (Col 3, Lines 58-67; Col 4, Lines 1-2).

As for claims 11 and 15, Sano in combination of Patterson already substantially disclose the claim as described above, but neither reference specifically discloses that the plurality of instructions are embodied in a NIC device driver associated with the NIC. However, there must be a NIC device driver program loaded into memory to be executed in order to control the operation of the NIC device, and Sano discloses the descriptors are implemented in software (Col 14, Lines 1-6). Therefore it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that Sano's software could be integrated with the NIC device driver program to simplify software management since their functions are related to the transfer and processing of packets in the computer system.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sano and Patterson, in further view of Muller et al. [US 6,389,468 B1] (hereinafter "Muller").

As for claim 5, Sano in combination of Patterson already substantially disclose the claim as described above, and Sano further discloses the first descriptor is 16 bytes long (Col 14, Lines 31-34) and the cache line is 32 bytes long (Col 11, Lines 66-68), but neither reference specifically discloses that the cache line is 64 bytes long. However, Muller discloses a similar computer system with descriptors where the descriptors are 16 bytes long and the cache line is 64 bytes line in order to allow efficient transfer of 4 descriptors in one transfer cycle. It would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that the width of the cache line is a design

choice, and having a 64 byte wide cache line as Muller's in place of Sano's 32 byte wide cache line enables 2 more 16 byte long descriptors to be transferred together.

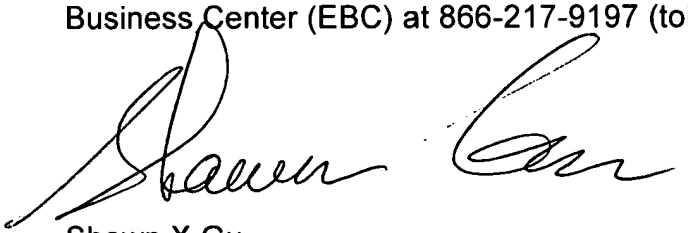
Mano Padmanabhan 7/6/06
MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571)272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Shawn X Gu
Assistant Examiner
Art Unit 2189

4 January 2006